Remarks

The non-final Office Action dated October 14, 2010, indicated that the previous allowability of claims 4, 6, and 14 was withdrawn, and further listed objections to claims 1, 10 and 14 with regard to informalities therein. The Office Action dated October 14, 2010, also listed the following new rejections under 35 U.S.C. § 103(a): claims 1, 3-10, 12 and 14-15 stand rejected over Tsuchi (US 2003/0160749) in view of Sakurai et al. (US 5,384,548); claims 11 and 13 stand rejected over the '749 reference in view of the '548 reference, and further in view of the Examiner's official notice; and claim 2 stands rejected over the '749 reference in view of the '548 reference, and further in view of Nishimura (US 2001/0004255). In this discussion set forth below, Applicant traverses each rejection without acquiescing to any averment in the Office Action, unless Applicant expressly indicates otherwise.

With regard to objections due to informalities in claims 1, 10 and 14, Applicant has amended the claims in accordance with the Examiner's suggestions to correct a spelling error and also improve readability with respect to reciting "An apparatus" instead of simply "Apparatus." Applicant appreciates the Examiner's suggestions, and understands that the objections are no longer applicable.

Each of the § 103(a) rejections fails because the Office Action has not established that the combination of the '749 and '548 references (upon which all rejections rely) teaches or suggests all claim limitations. For example, the Office Action does not assert that the references teach the claimed invention "as a whole" (§ 103(a)) including, *e.g.*, an input stage "configured to keep the ratio of the transconductance of the NMOS transistor doublet and the transconductance of the PMOS transistor doublet constant." As another example, the Office Action has failed to establish that the asserted "switches" are (or even could be) configured to operate in accordance with the secondary '548 reference's constant conductance operation and the related "concept" relied upon in the rejections. Because none of the cited references are represented as teaching these aspects, no reasonable combination of these references can provide correspondence. As such, the § 103 rejections fail.

Regarding the lack of correspondence to the claimed input stage, the Office Action has failed to establish that the switches in Figure 1 of the '749 reference (the

alleged "input stage") would be configured to keep the transconductance ratio of NMOS and PMOS transistors therein constant. The proposed modification of the cited circuit/switches of the '749 reference involves combining a "concept" in the '548 reference in which conductances of respective transistors are constant. However, the Office Action has not cited any circuit or other teaching that, if combined with the '749 reference, would cause the cited circuit in Figure 1 to maintain a transconductance ratio as asserted.

More specifically, the cited portion (Figure 10) of the secondary '548 reference is a plot showing the operation of a conductance stage that happens to have a region at which respective conductances (gmp, gmn) are both constant. Under such conditions, the ratio of the constant conductances is necessarily constant as well. However, the cited plot fails to disclose, teach or suggest any switches or other circuits that keep a transconductance ratio of NMOS and PMOS transistor doublets constant. Furthermore, there is no need to maintain any ratio, since the conductance of neither of the transistors varies under the cited operation. Accordingly, the '548 reference fails to disclose or even contemplate maintaining a constant transconductance *ratio* in the context of the claimed invention.

The rejections are further improper because the Office Action has provided no explanation as to how the '749 reference would be or could be modified to function as asserted, thus also failing to provide an (enabled) corresponding embodiment. While the Office Action asserts that Figure 10 in the secondary '548 reference allegedly teaches a concept of keeping the ratio of the transconductance of NMOS and PMOS transistor doublets constant, it fails to provide any explanation as to how the '749 reference would be modified to operate in accordance with the cited plots in the '548 reference. For example, the Office Action is silent as to how the cited "input stage" of the '749 reference would be or could be modified, with switches (as claimed) or otherwise, to arrive at any hypothetical embodiment that would correspond to the claimed invention. More specifically, the Office Action does not explain how the cited "plurality of switches" 111-120 in the '749 reference could be or would be configured with the '548 reference to maintain the transconductance ratio of the cited transistors 101, 102, 103 and 104 of the '749 reference constant.

In addition to the lack of teaching or suggestion of limitations directed to using switches to keep a transconductance ratio constant, it appears that the '548 reference requires a completely different kind of transconductance control. For example, column 4:39-56 of the '548 reference describes dynamically controlling bias currents to set transconductance, but fails to disclose or contemplate using switches to do so. It thus appears that the proposed combination of references would not employ any switches to control transconductance, and instead involves dynamic bias current control. This type of dynamic bias control further teaches away from any hypothetical embodiment in which switches are used in accordance with the claimed invention, as such switches would be ineffective in controlling a constant transconductance (issues with this teaching away are further discussed below).

Accordingly, the Office Action has failed to provide an operable embodiment that would correspond as asserted. The cited combination of references fails to teach or suggest the claimed invention as a whole, with respect to the above-discussed claim limitations (*e.g.*, as relevant to each of the independent claims). The rejections of the various dependent claims, such as those relating to the operation of switches to control a transconductance ratio, also fail to establish that the various switching connectivity would be configured to maintain such a ratio constant in accordance with the claimed invention (as a whole). For example, with specific regard to the rejection of claim 2, the Office Action's assertion that the '255 reference discloses "using gamma corrected picture signals" fails to provide any teaching or suggestion of limitations directed to switches that operate based upon the presence of positive or negative gamma data. Applicant therefore submits that the § 103(a) rejections of the independent claims, as well as all claims depending therefrom, are improper and should be removed.

Applicant further traverses the rejections of claims 11 and 13 over the '749 and '548 references "in further view of common knowledge" as the Office Action has relied upon a taking of "official notice" yet failed to establish that the allegedly "well known" subject matter was known in the art as required under § 103(a). Applicant thus traverses the Examiner's taking of Official Notice. For example, with respect to the rejection of claim 11, the Office Action has cited no reference that teaches an apparatus having an input stage circuit as claimed (*e.g.*, per the above), also having a source driver bank and a

bus for receiving input signals, that operates with a gate driver bank and an LCD panel. With respect to the rejection of claim 13, the Office Action has not cited teaching of an apparatus having an input stage circuit as claimed (*e.g.*, per the above), also having a source driver bank and a bus for receiving input signals as part of a panel module. Applicant thus cannot fully assess the merits of the rejection, as the Office Action has not established teaching of such a combination in the context of the claim, contrary to the requirements of a rejection under § 103. Moreover, the rejection does not evidence any consideration of the *Graham* factual inquires required by M.P.E.P. § 2141, and amounts to an unsupported assertion of obviousness, contrary to Supreme Court case law and M.P.E.P. § 2143.01. Accordingly the § 103(a) rejection of claims 11 and 13 are improper for these reasons and should be withdrawn. Should the rejections over the alleged "official notice" be maintained, Applicant respectfully requests evidence in support of the proposition that such teaching is well known in the prior art and any related explanation and/or evidence of motivation to combine this prior art with the main reference, consistent with M.P.E.P. § 2144.03. Applicant therefore requests that the rejections be removed.

Applicant further traverses the § 103(a) rejections because the Office Action fails to provide a proper reason for combining the cited references as asserted, and provides no explanation as to how the proposed combination could be made or as to why the result is "predictable," thus failing to comply with the requirements of M.P.E.P. § 2143.01, the 2010 U.S.P.T.O. *KSR* Guidelines, and authoritative case law.[1] For example, while the cited portions of the '548 reference (Figure 10) show a region of operation during which respective conductances happen to be constant, there is no disclosure, teaching or suggestion for maintaining the conductances constant, or of doing so in accordance with the asserted "input circuit" in the '749 reference. Further, while the Office Action asserts that the proposed combination would have been obvious "to obtain the predictable result of the ratio of the transconductance ... to be constant," it is silent as to how these results would be "predictable," particularly in consideration of the above discussion regarding the

[1] *See, e.g., KSR Int'l Co. v. Teleflex, Inc.*, 550 U.S. 398 (U.S. 2007)

Office Action's failure to explain how the '749 reference would be or could be modified to operate to maintain a constant transconductance ratio.

In addition, the Office Action's assertion that the proposed hypothetical embodiment involving the combination of references would involve "predictable results" fails to comply with the 2010 U.S.P.T.O. *KSR* Guidelines. Specifically, the requirements as consistent with the recent U.S.P.T.O. Guidelines specify that "[a]ny rationale employed must provide a link between the factual findings and the legal conclusion of obviousness," and also consistent with the *KSR* decision and M.P.E.P. § 2143.01."[2] As applicable here, the rejection fails to address any such factual findings regarding the allegations of "predictable results," much less any modification of the '749 reference to arrive at any corresponding hypothetical embodiment.

In view of the above, the asserted motivation does not address the actual combination at hand, and fails to comply with the requirements of the 2010 U.S.P.T.O. KSR Guidelines. There is therefore no motivation to combine references as asserted, and the rejections should be removed.

Applicant further submits that the § 103(a) rejections are improper for lack of motivation because the resulting (hypothetical) embodiment would appear to be inoperable in accordance with the '749 reference and/or the claimed invention, contrary to the M.P.E.P. and relevant law (a § 103(a) rejection cannot be maintained when the asserted modification undermines purpose of the main reference).[3] As consistent with the above discussion, the '548 reference requires dynamic control of bias currents in order to effect a constant transconductance (*see*, *e.g.*, column 4:39-56). Accordingly, combining the '548 reference with the '749 reference would appear to render the use of any switches (including cited "plurality of switches" 111-120) inoperable for maintaining any transconductance ratio, and instead requires the addition of a dynamic bias current control circuit. Applicant further notes that the Office Action is silent as to the addition of any such control circuit with the '749 reference or any resulting embodiment. Accordingly, the § 103(a) rejections are also improper because the cited references teach away from the proposed hypothetical embodiment.

---

[2] *See KSR at* 417 (U.S. 2007)
[3] *See In re Gordon*, 733 F.2d 900 (Fed. Cir. 1984)

Applicant further traverses the § 103(a) rejections because the cited references teach away from the Office Action's proposed combination. Consistent with the recent *KSR* decision, M.P.E.P. § 2143.01 explains the long-standing principle that a § 103 rejection cannot be maintained when the asserted modification undermines either the operation or the purpose of the main reference - the rationale being that the prior art teaches away from such a modification. *See KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 417 (U.S. 2007) ("[W]hen the prior art teaches away from combining certain known elements, discovery of a successful means of combining them is more likely to be non-obvious."). Applicant submits that the proposed combination would render the hypothetical embodiment (corresponding to the Office Action's proposed combination) inoperable because it would involve controlling transconductance using the dynamic bias control of the '548 reference, rather than switches. Moreover, the cited switches in the primary '749 reference would be inoperable for the purpose of the Office Action's proposed embodiment, as the '548 reference already controls transconductance using dynamic bias. Accordingly, there is no motivation to combine the references as asserted.

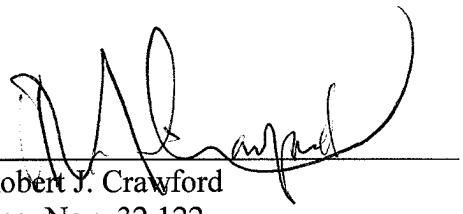
Applicant has amended claim 10 to remove its dependence upon claim 1. Applicant has also added new claims 16-17, and believes that these new claims are allowable over the cited combination of references for reasons including those discussed above. Applicant further believes that the cited combination of references fails to disclose, teach or suggest limitations directed to a plurality of switches that selectively direct input signals to a differential input and to connect another differential input to a reference voltage, to keep transconductance ratios of the NMOS and PMOS transistor doublets constant. Support for these claims may be found throughout the specification and figures, with exemplary embodiments shown in Figure 6 and described in connection therewith at pages 10:14-11:27. Per the Examiner's request, Applicant's undersigned representative telephoned the Examiner to discuss these and other amendments as presented herein (leaving a message). Should the Examiner have any questions regarding these or other amendments as discussed herein, a return telephone call to the undersigned is invited.

In view of the above, Applicant believes that each of the rejections has been overcome and the application is in condition for allowance. Should there be any remaining issues that could be readily addressed over the telephone, the Examiner is asked to contact the attorney/agent overseeing the application file, David Schaeffer, of NXP Corporation at (212) 876-6170 (or the undersigned).

Please direct all correspondence to:

Corporate Patent Counsel
NXP Intellectual Property & Standards
1109 McKay Drive; Mail Stop SJ41
San Jose, CA 95131

CUSTOMER NO. 65913

By: 

Robert J. Crawford
Reg. No.: 32,122
Eric J. Curtin
Reg. No. 47,511
651-686-6633
(NXPS.593PA)